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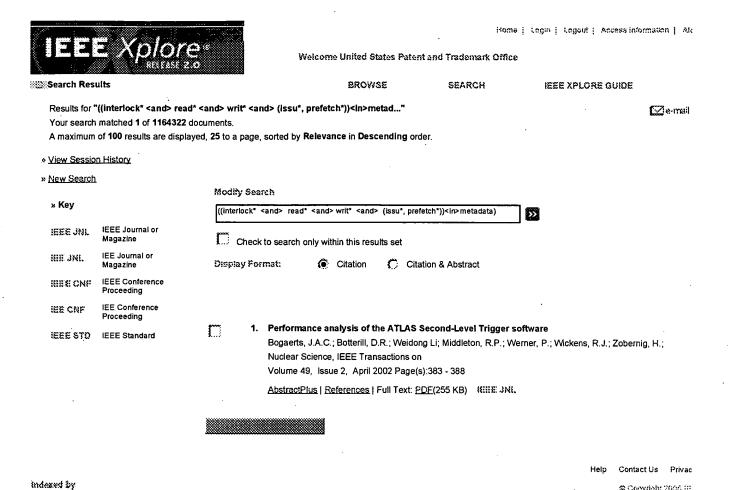
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<u>L20</u>	L18 and 15	21	<u>L20</u>
<u>L19</u>	L18 and 14	130	<u>L19</u>
<u>L18</u>	12 and prefetch\$5	253	<u>L18</u>
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<u>L15</u>	13 and 17	6	<u>L15</u>
<u>L14</u>	13 and 16	0	<u>L14</u>
<u>L13</u>	13 and 15	1	<u>L13</u>
<u>L12</u>	13 and 14	6	<u>L12</u>
<u>L11</u>	12 and L7	176	<u>L11</u>

<u>L10</u>	l2 and L6	1	<u>L10</u>
<u>L9</u>	12 and L5	77	<u>L9</u>
<u>L8</u>	12 and L4	250	<u>L8</u>
<u>L7</u>	(712/215-248)![CCLS]	6277	<u>L7</u>
<u>L6</u>	(711/155)[CCLS]	182	<u>L6</u>
<u>L5</u>	(711/147-169)[CCLS]	9919	<u>L5</u>
<u>L4</u>	(712/2-300)[CCLS]	10993	<u>L4</u>
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<u>L3</u>	L2 and (interlock\$6) near15 (read\$3 or writ\$6)	23	<u>L3</u>
<u>L2</u>	L1 and (recover\$6 or resum\$6) near5 address\$4	1328	<u>L2</u>
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				AbstractPlus Full Text: PDE (356 KB) IEEE CNF		
		n	2.	Relating buffer-oriented microarchitecture validation to high-level pipeline functionality Utamaphethai, N.; Blanton, R.D.; Shen, J.P.; High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IEEE International 7-9 Nov. 2001 Page(s):3 - 8		
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			3.	Design considerations and implementations of a high performance dynamic register file Joshi, R.V.; Hwang, W.; VLSI Design, 1999. Proceedings. Twelfth International Conference On 7-10 Jan. 1999 Page(s):526 - 531		
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		D	4.	Performance analysis of the ATLAS Second-Level Trigger software Bogaerts, J.A.C.; Botterill, D.R.; Weidong Li; Middleton, R.P.; Werner, P.; Wickens, R.J.; Zobernig, H.; Nuclear Science, IEEE Transactions on Volume 49, Issue 2, April 2002 Page(s):383 - 388		
		•		AbstractPlus References Full Text: PDF(255 KB) ISSE JNL		
			5.	A personal computer-based monitoring and control system for electron accelerators Van Ausdeln, L.A.; Haskell, K.J.; Jones, J.L.; Particle Accelerator Conference, 2001. PAC 2001. Proceedings of the 2001 Volume 2, 18-22 June 2001 Page(s):828 - 830 vol.2		
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